

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Appellant	:	Shinji Kuno	
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APPEAL BRIEF

Dear Sir:

Appellant submits, the following Appeal Brief pursuant to 37 C.F.R. § 41.37 for consideration by the Board of Patent Appeals and Interferences. Please charge any additional fees or credit any overpayment to our deposit Account No.02-2666.

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I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Kabushiki Kaisha Toshiba.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to Appellant, Appellant's legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-3, 18-20, 22-34 and 37-38 of the present application are pending. Claims 1-3, 18-20 and 22-38 were rejected under 35 U.S.C. §103. In accordance with 37 C.F.R. §41.33(b)(2), an Amendment has been filed concurrently with the filing of this Appeal Brief. This Amendment cancels claims 35-36 without prejudice and amends claims 19, 37 and 38. Appellant hereby appeals the outstanding rejection as applied to claims 1-3, 18-20, 22-34 and 37-38.

IV. STATUS OF AMENDMENTS

On January 23, 2009, the USPTO issued a Final Office Action. On March 13, 2009, Appellant filed a response to the Final Office Action. In response to the arguments set forth in the Final Office Action, the Examiner issued a non-final Office Action mailed April 9, 2009. In response to receipt of the non-Final Office Action, Appellant filed a response on August 7, 2009. On November 24, 2009, the Examiner issued a Final Office Action. As permitted by 37 C.F.R. §41.33(b)(2), claims 35-36 have been cancelled without prejudice and claims 19, 37 and 38 have been amended.

V. SUMMARY OF CLAIMED SUBJECT MATTER

1. INDEPENDENT CLAIMS 1, 19 AND 28

Independent claim 1 recites: An apparatus comprising:

a drive device (FIG. 2, element 117; page 9, line 6);

a communication bus (FIG. 2, element 100; page 9, lines 19-21);

a first processor (FIG. 2, element 111) coupled to the communication bus, the first processor to (i) receive a first stream data including video data and audio data routed over the communication bus and (ii) decode the first stream data (page 9, lines 17-21; page 14, lines 6-18);

a second processor (FIG. 2, element 115) provided with a second stream data including video data and audio data that is received from the drive device without being routed over the communication bus (page 12, lines 2-4), the second processor to decode the second stream data to reproduce the second stream data in accordance with an instruction sent from the first processor over the communication bus (page 12, lines 23-26; page 13, lines 2-5; page 14, lines 18-21).

Independent claim 19 recites: An apparatus comprising:

a drive device (FIG. 2, element 117; page 9, line 6);

a communication bus (FIG. 2, element 100; page 9, lines 19-21);

a first processor (FIG. 2, element 111) coupled to the communication bus, the first processor to decode a first stream data including video data and audio data routed over the communication bus (page 9, lines 17-21; page 14, lines 6-18);

a second processor (FIG. 2, element 115) provided with a second stream data including video data and audio data that is received from the drive device without being routed over the communication bus (page 12, lines 2-4), the second processor to decode the second stream data to reproduce the second stream data in accordance with an instruction sent from the first processor over the communication bus (page 12, lines 23-26; page 13, lines 2-5; page 14, lines 18-21); and

a network control unit (FIG. 2, element 118 and/or 119) coupled to the communication bus, the network control unit to transmit the first stream data via the communication bus (page 15, lines 25-27; page 16, lines 1-2).

Independent claim 28 recites: An apparatus comprising:

a communication bus (FIG. 2, element 100; page 9, lines 19-21);

a drive device (FIG. 2, element 117; page 9, line 6);

a video terminal (FIG. 2, element 300);

a first processor (FIG. 2, element 111) coupled to the communication bus, the first processor to (i) receive a first stream data including video data and audio data sent over the communication bus and (ii) decode the first stream data (page 9, lines 17-21; page 14, lines 6-18); and

a second processor (FIG. 2, element 115) coupled to the drive device, the video terminal and the first processor, the second processor being provided with a second stream data including video data and audio data that is sent from the drive device without use of the communication bus (page 12, lines 2-4), the second processor to (i) decode the second stream data for reproducing the second stream data in accordance with an instruction sent from the first processor via the communication bus (page 12, lines 23-26) and (ii) display video signals, that are based on the decoded first stream data and transmitted by the first processor over a video bus separate from the communication bus, on the video terminal (page 13, lines 2-5).

2. DEPENDENT CLAIMS 2-3, 18, 20, 22-27, 29-34 AND 37-38:

Dependent claim 2 recites: The apparatus according to claim 1, wherein the second processor is a stream processor (FIG. 2, element 115).

Dependent claim 3 recites: The apparatus according to claim 1, wherein the first processor is a central processing unit (CPU) (FIG. 2, element 111; page 9, lines 4-5 and 9-13).

Dependent claim 18 recites: The apparatus according to claim 1, wherein the drive device is a hard disk drive (FIG. 2, element 117; page 9, lines 6-7; page 13, lines 14-18).

Dependent claim 20 recites: The apparatus according to claim 19, wherein the network control unit includes an IEEE 1394 processor (FIG. 2, element 119).

Dependent claim 22 recites: The apparatus according to claim 1, wherein the communication bus is a Peripheral Component Internet (PCI) bus (FIG. 2, element 100).

Dependent claim 23 recites: The apparatus according to claim 1, further comprising:

a video bus (FIG. 2, element 103); and

a graphic controller (FIG. 2, element 201) in communication with the first processor and the second processor, the graphic controller to convert the decoded first stream data into display video signals (page 14, lines 11-14) and to transmit the display video signals to the second processor over the video bus (page 14, lines 14-21).

Dependent claim 24 recites: The apparatus according to claim 23, wherein the second processor superposes the display video signals transmitted over the video bus on a video image generated from the decoded second stream data in accordance with display information transferred from the first processor to the second processor over the communication bus (page 24, lines 2-19).

Dependent claim 25 recites: The apparatus according to claim 24, wherein the display information includes information designating a region in a drawing area and a transparency rate at the display video signals on a screen (page 24, lines 15-19).

Dependent claim 26 recites: The apparatus according to claim 1, further comprising:

a television tuner adapted to transmit a third stream data to the second processor for storage into a storage medium associated with the drive device (page 10, lines 4-6).

Dependent claim 27 recites: The apparatus according to claim 1, further comprising:

a television tuner (FIG. 2, element 114; page 9, line 6); and

a transport stream bus coupled to the television tuner and the second processor (FIG. 2, element 101; page 10, lines 1-3), the transport stream bus enables transmission of the third stream data to the second processor without using the communication bus (page 10, lines 4-6).

Dependent claim 29 recites: The apparatus according to claim 28, wherein the second processor superposes the display video signals on a video image generated from the decoded second stream data in accordance with display information transferred from the first processor to the second processor through the communication bus (page 24, lines 2-19).

Dependent claim 30 recites: The apparatus according to claim 29, wherein the display information includes information designating a region in a drawing area and a transparency rate at the display video signals on a screen (page 24, lines 15-19).

Dependent claim 31 recites: The apparatus according to claim 1, wherein the first stream data is received from a first source and the second stream of data is received from a second source different than the first source (page 15, lines 6-8; page 10, lines 4-6).

Dependent claim 32 recites: The apparatus according to claim 31, wherein the first stream data is received via a connector being different than the second source being a drive device (FIG. 2, elements 302 and 303; page 15, lines 1-9; page 12, lines 23-28).

Dependent claim 33 recites: The apparatus according to claim 28, wherein the first stream data is received from a source different than the drive device (page 12, lines 23-26; page 15, lines 1-9).

Dependent claim 34 recites: The apparatus according to claim 28, wherein the first stream data is received from the source being one of a network processor and an IEEE 1394 processor (page 15, lines 1-9; page 16, lines 1-3).

Dependent claim 37 recites: The apparatus according to claim 19, wherein the communication bus comprises a Peripheral Component Interconnect (PCI) bus (FIG. 2, element 100).

Dependent claim 38 recites: The apparatus according to claim 28, wherein the communication bus comprises a Peripheral Component Interconnect (PCI) bus (FIG. 2, element 100).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

- A. Claims 1-3, 18 and 31-32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higashida in view of Cloutier.
- B. Claims 28-30 and 33-34 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higashida in view of Cloutier.

- C. Claims 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higashida in view of Cloutier.
- D. Claims 22-27, 37 and 38 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higashida in view of Cloutier.

VII. ARGUMENTS

A. The combined teachings of Higashida and Cloutier do not disclose all of the elements as recited in independent claim 1, and thus, the corresponding rejection is improper

Claims 1-3, 18 and 31-32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higashida (U.S. Patent No. 6,862,401) in view of Cloutier (U.S. Patent No. 5,847,771). Appellant respectfully traverses the rejection because a *prima facie* case of obviousness has not been established.

As the Examiner is aware, to establish a *prima facie* case of obviousness, the prior art references, when combined, must teach or suggest all of the claim limitations. *See MPEP §2143; see also In Re Fine, 873 F. 2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)*. In particular, the Supreme Court in *Graham v. John Deere*, 383 U.S. 1, 148 USPQ 459 (1966), stated: “Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined.” *MPEP §2141*. In *KSR International Co. vs. Teleflex, Inc.*, 127 S.Ct. 1727 (2007) (Kennedy, J.), the Court explained that “[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, *all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.*” *Emphasis added*. The Court further required that an explicit analysis for this reason must be made. “[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *KSR 127 S.Ct.* at 1741, quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

In the instant case, Appellant respectfully submits that the teachings of the combined references do not suggest all of the claim limitations set forth in independent claim 1. Also, there are significant differences between the cited references and the claimed invention with no apparent reason to combine known elements in the manner as claimed. Thus, no *prima facie* case of obviousness has been established.

For instance, the Examiner interprets the first stream of data as the file management information (13) described in Higashida. *See page 4 of the Final Office Action dated 11/24/09*. In addition, the Examiner Action interprets the “drive device” as the hard disk (8) of Higashida; the “second processor” as the recording/reproducing control means (7) of Higashida; and the “second stream data” as the MPEG2 stream data from an IEEE 1394 interface (6) in Higashida. *See page 4 of the Final Office Action dated 11/24/09*.

Based to this interpretation, the teachings of the combined references do not suggest all of the claim limitations because, where the “second stream data” is considered to be the MPEG2 stream data from an IEEE 1394 interface (6) in Higashida, the second stream data is not received from the drive device as claimed. Thus, by this fact alone, a *prima facie* case of obviousness has not been established.

Additionally, based to the above-described interpretation, Appellant respectfully submits that a *prima facie* case of obviousness cannot be established because the file management information (interpreted by the Examiner as the “first stream of data”) does not include any audio and video data as explicitly claimed. The Examiner acknowledges that file management information is not video and audio data. *See page 5 of the Final Office Action dated 11/24/09*. However, the Examiner alleges that the teaching of a video and audio stream (subset of the MPEG2 video signal) in Cloutier, combined with the teachings of Higashida, would render the claimed invention obvious. *See page 5 of the Final Office Action dated 11/24/09*. We disagree because (1) the teachings of these references provide no basis for any combination as alleged, and (2) the combination would render the claimed invention of Higashida inoperable.

First, when determining the patentability of a claimed invention which combined two known elements, “the question is whether there is something in the prior art as a

whole suggest the desirability, and thus the obviousness, of making the combination.” *In re Beattie*, 974 F.2d 1309, 1312 (Fed. Cir. 1992), 24 USPQ2d 1040; *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). Higashida describes the storage of file management information (13), which includes information called a file allocation table (FAT) and a directory. *See col. 5, lines 5-7 of Higashida*. The file management information (13) is crucial information for the recording apparatus (1) because it “tells in which order data are stored in which recording blocks of the hard disk 8 as files.” *See col. 4, lines 63-65 of Higashida*. Hence, the prior art references as a whole fail to suggest the desirability, and thus the obviousness, of the file management information being substituted with video and audio.

Moreover, Higashida is specifically directed to a recording apparatus that provides persistent storage of the file management information in lieu of non-persistent storage within main memory. *See col. 1, line 57 - col. 2, line 4 of Higashida*. However, the modification or combination of the prior art as proposed by the Examiner, namely the alteration of the file management information as video and audio, would change the principle of operation of the recording apparatus. Hence, this combination is improper because, according to well-established U.S. patent prosecution principles, if the proposed modification or combination of the prior art would change the principle of operation of the prior invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Second, even presuming that there was an apparent reason for combining the above-described teachings of Highashida and Cloutier, the recording apparatus of Higashida modified based on the teachings of Cloutier would be inoperable. The Federal Circuit has firmly established that, if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose (i.e. persistent storage of file management information 13 needed for ordering of data in the recording blocks), then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). The substitution of the file

management information for the video and audio of Cloutier would render the recording apparatus of Higashida unsatisfactory for its intended purpose.

Hence, in light of the foregoing, Appellant respectfully requests that the Examiner withdraw the §103(a) rejection as applied to independent claim 1 and those claims dependent thereon.

B. The combined teachings of Higashida and Cloutier do not disclose all of the elements as recited in independent claim 28, and thus, the corresponding rejection is improper

Claims 28-30 and 33-34 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higashida in view of Cloutier. Appellant respectfully traverses the rejection because a *prima facie* case of obviousness has not been established. Appellant incorporates the arguments set forth above in section VII(A) and further submits that the combined teachings of Higashida and Cloutier do not describe or suggest a first processor to *decode the first stream data* (i.e. the file management information) or a second processor (recording/reproducing control means 7) to *decode the second stream data for reproducing the second stream data in accordance with an instruction sent from the first processor* via the communication bus. *Emphasis added.*

More specifically, with respect to independent claim 28, the Examiner alleges that the reading of the file management information by the CPU, as described in col. 5, lines 45-60 of Higashida, discloses a decode of the first stream data. Appellant respectfully disagrees that the reading of data from a hard disk drive constitutes a “decode” operation as claimed. Rather, Appellant respectfully points out that this strained interpretation merely exemplifies impermissible hindsight reconstruction that has been performed during this examination.

Furthermore, the Examiner alleges that col. 6, lines 54-65 of Higashida discloses a decode of the second stream data (AV data) for reproducing the second stream data in accordance with an instruction sent from the first processor. Appellant disagrees because the cited section of Higashida is directed to an instruction transmitted from the CPU (11) to *control the writing* of the AV data into continuous subsequent recording blocks. This cited section is not directed to the decode of the second stream data *sent from the drive device* (i.e. the hard disk per Examiner).

Therefore, Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness and respectfully requests the Examiner to withdraw the outstanding §103 rejection as applied to independent claim 28 and those claims dependent thereon.

C. The combined teachings of Higashida and Cloutier do not disclose all of the elements as recited in independent claim 19, and thus, the corresponding rejection is improper

Claims 19 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higashida in view of Cloutier. Appellant respectfully traverses the rejection because a *prima facie* case of obviousness has not been established. Appellant incorporates the arguments set forth above in section VII(A) and further submits that the combined teachings of Higashida and Cloutier do not describe or suggest a network processor to a network control unit *coupled to the communication bus and to transmit the first stream data via the communication bus. Emphasis added.*

More specifically, the Examiner alleges that the teachings of Higashida, when combined with the teachings of a network interface module (NIM 50) shown in FIG. 5 of Cloutier, renders the claimed invention obvious. Appellant respectfully disagrees. First, it is unclear how the NIM 50 could be coupled to the “communication bus,” which is alleged by the Examiner to be the bus between the CPU (11) and the recording/reproducing control means (7) of Higashida. Furthermore, given that the NIM 50 of Cloutier is an interface module for a network, it would not be involved in the transmission of the first stream (i.e. the file management information per the Examiner) from a hard disk drive, which is an internal component within the recording apparatus (1). Appellant respectfully asserts that this strained interpretation yet again exemplifies impermissible hindsight reconstruction that has been performed during this examination of the subject application.

Thus, Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness and respectfully requests the Examiner to withdraw the outstanding §103 rejection as applied to independent claim 19 and claim 20 dependent thereon.

D. The combined teachings of Higashida and Cloutier do not disclose all of the elements as recited in dependent claims 22-27, 37 and 38, and thus, the corresponding rejection is improper

Claims 22-27, 37 and 38 are rejected under 35 U.S.C. §103(a) as being unpatentable over Higashida in view of Cloutier. Appellant respectfully traverses the rejection because a *prima facie* case of obviousness has not been established. Appellant incorporates the arguments set forth in section VII(A) above and further submits that the combined teachings of Higashida and Cloutier do not describe or suggest the communication bus being a Peripheral Component Interconnect (PCI) bus as set forth in dependent claims 22, 37 and 38.

More specifically, the Examiner alleges that the combined teachings of the cited references, most notably col. 13, lines 9-14 of Higashida, disclose the communication bus as being a PCI bus. Appellant respectfully disagrees. As stated above, the Examiner considers the “communication bus” as the bus between the recording/reproducing control means (7) and the CPU (11). *See page 4 of the Final Office Action dated 11/24/09; see FIG. 2 of Higashida.* However, col. 13, lines 9-14 of Higashida discusses the potential substitution of the IEEE 1394 bus (5) of FIG. 1, namely the bus *external* to the recording apparatus (1) that is used for coupling to the set-top box (2), with a PCI bus. *Emphasis added.* In accordance with such teachings, in contrast to the Examiner’s allegations, there is no description or suggestion of the bus between the recording/reproducing control means (7) and the CPU (11) being a PCI bus.

Thus, Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness and respectfully requests the Examiner to withdraw the outstanding §103 rejection as applied to dependent claims 22-27 and 37-38.

VIII. CONCLUSION

Appellant respectfully requests that the Board enter a decision overturning the Examiner's rejections.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: February 24, 2010

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IX. CLAIM APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (Previously Presented) An apparatus comprising:
a drive device;
a communication bus;
a first processor coupled to the communication bus, the first processor to (i) receive a first stream data including video data and audio data routed over the communication bus and (ii) decode the first stream data;
a second processor provided with a second stream data including video data and audio data that is received from the drive device without being routed over the communication bus, the second processor to decode the second stream data to reproduce the second stream data in accordance with an instruction sent from the first processor over the communication bus.
2. (Previously Presented) The apparatus according to claim 1, wherein the second processor is a stream processor.
3. (Previously Presented) The apparatus according to claim 1, wherein the first processor is a central processing unit (CPU).
- 4-17. (Cancelled).
- 18 (Previously Presented) The apparatus according to claim 1, wherein the drive device is a hard disk drive.
19. (Previously Presented) An apparatus comprising:
a drive device;
a communication bus;
a first processor coupled to the communication bus, the first processor to decode a first stream data including video data and audio data routed over the communication bus;

a second processor provided with a second stream data including video data and audio data that is received from the drive device without being routed over the communication bus, the second processor to decode the second stream data to reproduce the second stream data in accordance with an instruction sent from the first processor over the communication bus; and

a network control unit coupled to the communication bus, the network control unit to transmit the first stream data via the communication bus.

20. (Previously Presented) The apparatus according to claim 19, wherein the network control unit includes an IEEE 1394 processor.

21. (Cancelled).

22. (Previously Presented) The apparatus according to claim 1, wherein the communication bus is a Peripheral Component Interconnect (PCI) bus.

23. (Previously Presented) The apparatus according to claim 1, further comprising:
a video bus; and

a graphic controller in communication with the first processor and the second processor, the graphic controller to convert the decoded first stream data into display video signals and to transmit the display video signals to the second processor over the video bus.

24. (Previously Presented) The apparatus according to claim 23, wherein the second processor superposes the display video signals transmitted over the video bus on a video image generated from the decoded second stream data in accordance with display information transferred from the first processor to the second processor over the communication bus.

25. (Previously Presented) The apparatus according to claim 24, wherein the display information includes information designating a region in a drawing area and a transparency rate at the display video signals on a screen.

26. (Previously Presented) The apparatus according to claim 1, further comprising:
a television tuner adapted to transmit a third stream data to the second processor for storage into a storage medium associated with the drive device.

27. (Previously Presented) The apparatus according to claim 1, further comprising:

a television tuner; and

a transport stream bus coupled to the television tuner and the second processor, the transport stream bus enables transmission of the third stream data to the second processor without using the communication bus.

28. (Previously Presented) An apparatus comprising:

a communication bus;

a drive device;

a video terminal;

a first processor coupled to the communication bus, the first processor to (i) receive a first stream data including video data and audio data sent over the communication bus and (ii) decode the first stream data; and

a second processor coupled to the drive device, the video terminal and the first processor, the second processor being provided with a second stream data including video data and audio data that is sent from the drive device without use of the communication bus, the second processor to (i) decode the second stream data for reproducing the second stream data in accordance with an instruction sent from the first processor via the communication bus and (ii) display video signals, that are based on the decoded first stream data and transmitted by the first processor over a video bus separate from the communication bus, on the video terminal.

29. (Previously Presented) The apparatus according to claim 28, wherein the second processor superposes the display video signals on a video image generated from the decoded second stream data in accordance with display information transferred from the first processor to the second processor through the communication bus.

30. (Previously Presented) The apparatus according to claim 29, wherein the display information includes information designating a region in a drawing area and a transparency rate at the display video signals on a screen.

31. (Previously Presented) The apparatus according to claim 1, wherein the first stream data is received from a first source and the second stream of data is received from a second source different than the first source.

32. (Previously Presented) The apparatus according to claim 31, wherein the first stream data is received via a connector being different than the second source being a drive device.

33. (Previously Presented) The apparatus according to claim 28, wherein the first stream data is received from a source different than the drive device.

34. (Previously Presented) The apparatus according to claim 28, wherein the first stream data is received from the source being one of a network processor and an IEEE 1394 processor.

35. (Cancelled).

36. (Cancelled).

37. (Previously Presented) The apparatus according to claim 19, wherein the communication bus comprises a Peripheral Component Interconnect (PCI) bus.

38. (Previously Presented) The apparatus according to claim 28, wherein the communication bus comprises a Peripheral Component Interconnect (PCI) bus.

X. EVIDENCE APPENDIX

None

XI. RELATED PROCEEDINGS APPENDIX

None